

Designed Implementation of Modified Area Efficient Enhanced Square Root Carry Select Adder

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ABSTRACT

In the design of Integrated Circuits, area occupancy plays a vital role because of increasing the necessity of portable systems. Carry Select Adder (CSLA) is one of the fastest adders used in many data-processing processors to perform fast arithmetic functions. In this paper, an area-efficient carry select adder by sharing the common Boolean logic term (CBL) with BEC is proposed. After logic simplification and sharing partial circuit, only one XOR gate and one inverter gate in each summation operation as well as one AND gate and one inverter gate in each carry-out operation are needed. Based on this modification a new modified 32-Bit Square-root CSLA (SQRT CSLA) architecture has been developed. The modified architecture has been developed using Common Boolean Logic(CBL). The proposed architecture has reduced area, power and delay.

Keywords —Area efficient, Square-root CSLA (SQRT CSLA), Common Boolean Logic (CBL), Binary to Excess-1 CONVERTER(BEC).

1. INTRODUCTION

Design of area- and power-efficient high-speed data path logic systems are one of the most substantial areas of research in VLSI system design. In digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next position. The CSLA is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum.

However, the Regular CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input $C_{in}=0$ and $C_{in}=1$. then the final sum and carry are selected by the multiplexers (mux).

The basic idea of this work is to use Binary to Excess-1 Converter(BEC) sharing common Boolean logic term (CBL) instead of RCA with $C_{in}=1$ in the SQRT CSLA to achieve lower area and power consumption .The main advantage of this BEC logic comes from the lesser number of logic gates than the n-bit Full Adder (FA) structure.

2. RELATED WORK

A simple approach is proposed by B. Ramkumar and Harish M Kittur to reduce the area and power of SQRT CSLA architecture. The reduced number of gates of this work offers the great advantage in the reduction of area and also the total power. The compared results show that the modified SQRT CSLA has a slightly larger delay (only 3.76%), but the area and power of the 64-b modified SQRT CSLA are significantly reduced by 17.4% and 15.4% respectively. The power-delay product and also the area-delay product of the proposed design show a decrease for 16-, 32-, and 64-b sizes which indicates the success of the method and not a mere tradeoff of delay for

power and area. The modified CSLA architecture is therefore, low area, low power, simple and efficient for VLSI hardware implementation. [1]

HEMIMA.R, CHRISJIN GNANA SUJI.C proposed work uses a simple and efficient transistor level modification to significantly reduce the area and power of the CSLA. Based on this modification 4-bit CSLA architecture have been developed and compared with the regular CSLA architecture. In this proposed architecture RCA was designed using four bit 8T full adder. The multiplexer used in this block was designed with 2T. By reducing the number of transistors used the performance parameters, area and power reduces with slight increase in delay.[2]

Due to importance of adders in signal processing Authors Habib Ghasemizadeh Tamar, Akbar Ghasemizadeh Tamar designed a High Speed Area Reduced 64-bit Static Hybrid Carry-Lookahead/Carry-Select Adder. Combination of logic styles is an attractive approach for improvement of digital circuits. In this design we used combination of conventional CMOS (C-CMOS) and transmission gate (TG) logic to decrease critical path delay of adder. So with small hardware this adder can operate in very high speed.[3]

Shivani Parmar, Kirat Pal Singh proposed the efficient modified Carry Select Adder (CSA) of 8-bit, 16-bit, 32-bit by using a single Ripple Carry Adder (RCA). The selection of ripple carry adder gives the specifications by accurate resource estimation. The high speed carry select adder performs binary addition pervasive in FPGA applications. Modified carry select adder shows performance and resource improvements as compared with conventional carry select adder. The frequency of conventional CSA is better than modified CSA. This paper proposes a scheme which reduces the delay, area and power than conventional CSA. The overall improvement in Modified Sqrt CSLA shows better results in terms of area power and delay. Hence, proposed modified Sqrt CSLA is being used for power and area efficient devices.[4]

To achieve more speed CSLA is replaces by Sqrt CSLA. The CSLA is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum [5]-[6]. However, the CSLA is not area efficient

because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry input $C_{in}=0$ and $C_{in}=1$, the final sum and carry are selected by the multiplexers(mux) [7]-[8]. Therefore in stead of Ripple Carry Adder Binary Excess-1 Converter(BEC) with sharing common Boolean Logic(CBL) concept is used.

3. PROPOSED WORK

The main idea of this work is to use BEC instead of the RCA with $C_{in}=1$ in order to reduce the delay and area utilization of the regular Sqrt CSLA. To replace the n-bit RCA, a n+1 bit BEC is required [2] this structure one input of the 8:4 mux gets as it input (B3, B2, B1, and B0) and another input of the mux is the BEC output. This produces the two possible partial outputs in parallel according to the control signal C_{in} . The importance of the BEC logic stems from the large silicon area reduction when the CSLA with large number of bits are designed.

The modified 16-bit Sqrt CSLA using BEC is shown in Fig.1. The structure is again divided into five groups with different sizes of Ripple carry adder and BEC. The group2, group3, group4 and group5 of 16-bit Sqrt CSLA are shown in Fig.2. The parallel Ripple carry adder with $C_{in}=1$ is replaced with BEC. One input to the multiplexer goes from the RCA with $C_{in}=0$ and other input from BEC. Comparing the individual groups of both regular and modified Sqrt CSLA, it is clear that the BEC structure reduces delay. But the disadvantage of BEC method is that the area is increasing than the regular Sqrt CSLA. Once the carry-in signal is ready, then select the correct carry-out output according to the logic state of carry-in signal .

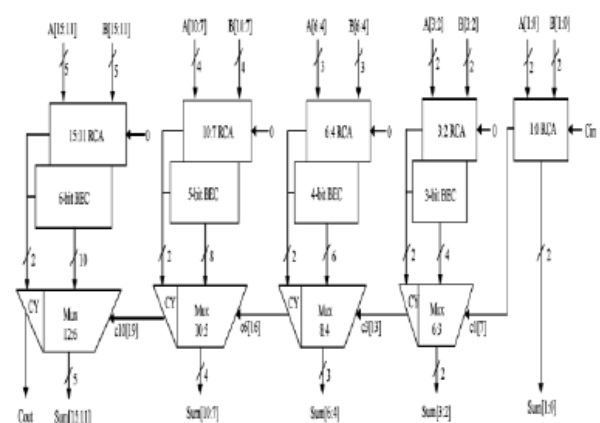


Fig.1 Modified 16 Bit Sqrt CSLA

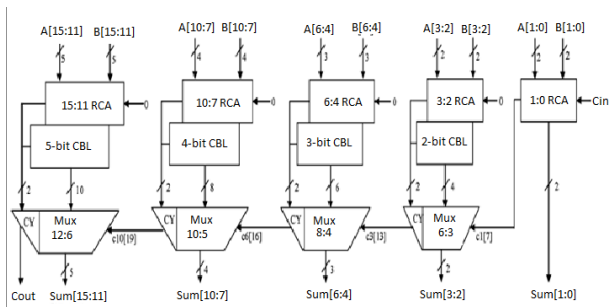


Fig.2 Proposed 16 Bit SQRT CSLA

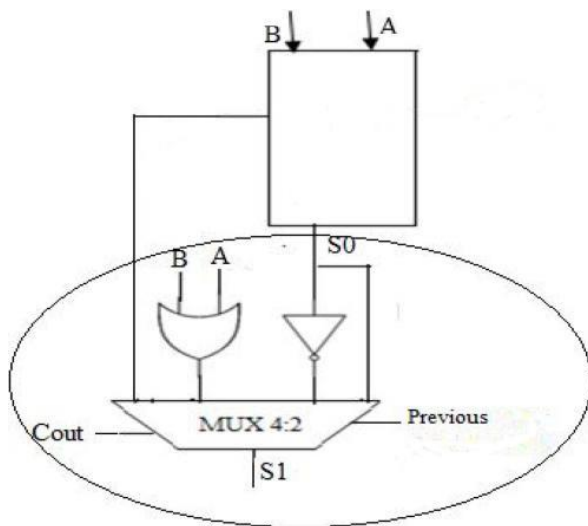


Fig.3 Single Bit CBL Full Adder

This method replaces the BEC add one circuit by Common Boolean Logic. The proposed 16-bit SQRT CSLA architecture is shown in Fig.2. The summation and carry signal for full adder which has $C_{in}=1$, generate by INV and OR gate. Through the multiplexer, the correct output result is selected according to the logic state of carry-in signal. The internal structure of the group3 of proposed CSLA is shown in Fig.2.

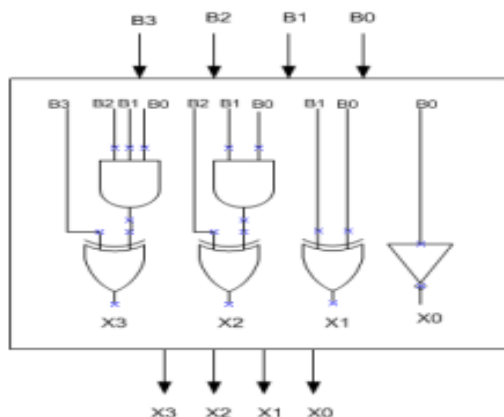


Fig.4 Structure of 4-bit BEC

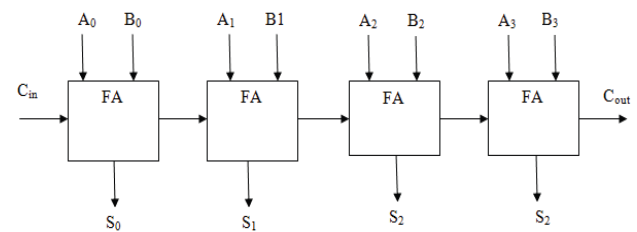


Fig.5 Block Diagram Of Ripple Carry Adder

In this proposed SQRT CSLA Ripple Carry Adder(RCA), Binary Excess-1 Converter(BEC) and Common Boolean Logic(CBL) this blocks are perform vital role in this architecture Fig.3 shows Common Boolean logic(CBL), Fig.4 shows Binary Excess-1 Converter(BEC) and Fig.5 shows block diagram of Ripple Carry Adder(RCA). From this design the 32-bit SQRT CSLA architecture has been designed.

3. OBJECTIVES

The primary objectives of this study can be summarized as, The 8-bit SQRT CSLA is done by the same structure of 16-bit SQRT CSLA except group4 and group5. The 8-bit inputs are directly given to the full adder to complete the 8-bit sum and carry. The 32-bit SQRT CSLA is done by cascading the two 16-bit SQRT CSLA. Table exhibit the delay and area of modified and proposed 32-bit SQRT CSLA. Simulation is carried out using Tanner Tool 13.1 EDA Tool.(Electronics Design Automation) as the target device and area can be verified by using simple formula from layouton Microwind Tool. The major disadvantage of modified architecture using BEC is increasing area. This disadvantage is overcome in the proposed architecture by sharing Common Boolean Logic (CBL) which reduces area than the regular and modified Square-root Carry select adder. The comparison chart between area, delay and logic levels is shown below:

TABLE-I

Parameters	Existing CSLA	Proposed CSLA
Power(μ w)	1127.3	969.9
Area(μ m ²)	4783	3985
Delay(ns)	5.137	5.482

Table-1: Comparison of 32-Bit SQRT CSLA.

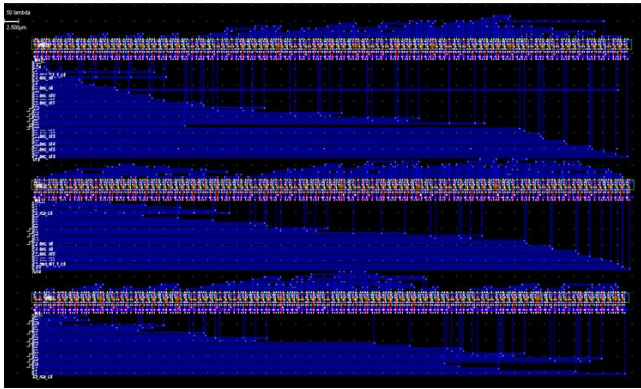


Fig-1: Layout of Area.

4. CONCLUSIONS

SQRT CSLA are significantly reduced, proposed design show a decrease for 16-b, 32-b sizes which indicates the success of the method and reduced delay ,power and area. The modified CSLA architecture is therefore, low area, low power, simple and efficient for VLSI hardware implementation. The regular SQRT CSLA has the disadvantage of occupying more chip area. The reduced number of gates of this work offers the great advantage in the reduction of area. This paper proposes a scheme which reduces the area than the regular and modified SQRT CSLA. It would be interesting to test the design of the 64 and 128 bit SQRT CSLA.

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