Design of a 1GHz Voltage Control Oscillator for PLL using 0.18µm CMOS Technology

Bharati D Mangrulkar¹, Tushar Uplanchiwar²

Bharati D Mangrulkar¹, Department of Electronics and Communication, Behind Bank of India Main Road Ekori ward Chandrapur Maharashtra India

bhartimangrulkar01@gmail.com

Prof. Tushar Uplanchiwar², Department of Electronics and Communication, Nagpur Maharashtra India
tushar.ece@tgpcet.com

ABSTRACT

This paper presents a design technique of efficient wide frequency range voltage control oscillator (VCO). An implementation of five stage CMOS VCO in Tanner S-Edit environment with high oscillation frequencies for different input control voltage (D.C.) & low power consuming circuit with low W/L Ratio is proposed in this paper. For circuit simulation 180nm technology is used. This circuit gives different Oscillation from 0.5v to 1.0v at input control voltage ranges from 0.5 V to 1.0 V. Circuit simulation resulted average power consumption at 4.522 e-006.

Keywords: Power, Low W/L ratio, Voltage Control Oscillator (VCO), Phase lock loop (PLL).

1. INTRODUCTION

A phase locked loop abbreviated as PLL is a control system that generates an output signal whose phase is related to the phase of an input signal. While there are several different types, it is easy to initially visualize as an electronic circuit consists of voltage controlled oscillator and a phase detector. The oscillator generates a periodic signal, and a phase detector compares the phase of that signal with the phase of input periodic signal, adjusting the oscillator to keep the phases matched. Bringing the output signal back towards the input signal for comparison is called a feedback loop. Keeping the input and output phase in lock step also implies keeping the input and output frequencies the same. A Phase locked loop (PLL) is designed in feedback loop that helps to lock the on chip clock phase for an input clock or signal. A PLL are widely used in a digital circuit for clock generator as well as for timing recovery. For this purposes the high performance PLL are in demand. Although the clock generation in off-chip, reference frequency is limited for a crystal oscillator (Typically in several MHz). A PLL receives the clock and multiplies with several GHz operating frequency. Timing recovery pertains to the data communication between all parts of the chip. To satisfy the increase in on-chip processing rate it must increase data rate. The input data and the on-chip clock are not fixed. A PLL is a closed loop control system which compares both the input and output phase. High performance digital system are ought to clock for a sequential operation and synchronization between functional unit and ICs. Since there is rapid increase in data generation in processing technology and processor architecture, there is a necessity of high frequency clock generation. For this the well-known technology “Phase locked loop” is being admired.

2. SYSTEM OVERVIEW

The basic concept of Phase locking was being same since 1930s. However, the designing techniques of PLL with voltage control oscillator (VCO) are to be a challenging for the clock timing, power consumption and area. A PLL is a multiplier for a low frequency clock for producing high frequency clock. A PLL is a negative feedback control circuit. The overall significant of the PLL is to match the clock with
the feedback signal with phase mode. The PLL is continuously comparing the signal since they are in lock mode, the output becomes constant.

The PLL having five main blocks,

- Phase Detector
- Charge Pump
- Low Pass Filter
- Voltage Control Oscillator
- Divided by N Count

![Fig. 1. A block diagram of PLL](image1)

The phase frequency detector (PFD) is possible to error output signal based on the reference clock and feedback clock. If there is a phase difference between these two signals, then there is possibility for generation of up/down synchronized signal to the charge pump/low pass filter. If the error signal from the PFD is an up signal, then charge pumps charges the capacitor of low pass filter which decrease the control voltage. Control voltage is the input to the VCO. Thus LPF is necessary to allow DC signal to the VCO and also necessary to store the charge to charge pump. The purpose of VCO is to boost or slow the speed for charge pump.

A voltage controlled oscillator is an oscillator with an output signal whose output can be varied over a range which is controlled by input dc voltage. It is an oscillator whose output frequency is directly related to the voltage at its input. The oscillation frequency varies from few hertz to hundred Giga hertz by varying the input dc voltage.

Voltage control oscillator is the very essential block for the designing of RF transceiver for generation of local oscillation frequency to up and down convert the input signal. Oscillators generate periodic output sinusoidal signal.

The condition should be simultaneously satisfied for steady state oscillations,

- The loop gain \(|H(j\omega)| = 1\)
- The total phase shift around the loop must be 0° or 360°

### 3. VCO SCHEMATIC

The operation of VCO (Current Starved) is analogous to Ring VCO. The PMOS_1 and NMOS_2 act as an inverter with \(L=0.18\) and \(W=0.18\), while PMOS_6 and NOMS_10 act as current source with \(L=0.18\) and \(W=0.60\). We can find inverter as a current starved. PMOS_11 and NMOS_11 since the drain current \((I_D)\) control by the input control voltage.

The schematic representation of 5 stage current starved VCO is shown in Figure 2. It can be designed by cascading five inverters.

![Fig. 2. Schematic of 5 stages current starved VCO.](image2)

The size for figure 2 is being calculated as a total capacitance. The total capacitance \(C_T\) is given by formula,

\[
C_T = \frac{N \times C (W_{PMOS} \times W_{NMOS})}{2} \quad \text{(1)}
\]

Where,

- \(Co\) is oxide capacitance
- \(N\) is the number of cascade inverter.

In this work, involvement of capacitors are eliminated in order to reduce area of implementation and avoid distortion therefore total capacitance \(C_T\) is taken as unity i.e 1.

The drain current \((I_D)\) is calculated as

\[
I_D = N \times V_{DD} \times C_T \times F \quad \text{(2)}
\]

The oscillation frequency is given by

\[
F = \frac{1}{N \times T_D} \quad \text{(3)}
\]

Where, \(T_D\) is delay time.
4. SIMULATION AND OUTPUT

When the output of charge pump is applied to VCO it acts as a control signal to the five stage circuit and controls the output oscillations simultaneously. Output waveform is as shown in figure-3. It seen that the 1.858 GHz output frequency is generated for 1.0 V control voltage.

![Output waveform of VCO](image)

The output waveform of current starved VCO for control voltage 1.0V generates an output frequency of 1.858 GHz as shown in figure-3. The simulation results for Average power consumption for figure-2 is calculate in Tanner T-Spice is 4.522 e-006 Watt.

![Measurement of output frequency](image)

When the control voltage is varied from 0.5 V to 1.0 V the oscillation frequency is varying from 448.43 MHz to 1.858 GHz respectively as shown in table 1.

<table>
<thead>
<tr>
<th>Sr No.</th>
<th>Control Voltage (volts)</th>
<th>Output Frequency (Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.5</td>
<td>448.430 MHz</td>
</tr>
<tr>
<td>2</td>
<td>0.6</td>
<td>471.698 MHz</td>
</tr>
<tr>
<td>3</td>
<td>0.7</td>
<td>1.069 GHz</td>
</tr>
<tr>
<td>4</td>
<td>0.8</td>
<td>1.495 GHz</td>
</tr>
<tr>
<td>5</td>
<td>0.9</td>
<td>1.733 GHz</td>
</tr>
<tr>
<td>6</td>
<td>1.0</td>
<td>1.858 GHz</td>
</tr>
</tbody>
</table>

5. CONCLUSION

This paper presents the schematic of low power with output frequency 1.858 GHz current starved VCO using Tanner (S-Edit). The simulation of this project shows that the VCO could achieve high frequency of oscillation with low power consumption. This design may be compatible for PLL as a frequency multiplier. The efficient wide frequency VCO with low power consumption is successfully achieved.

REFERENCES


[3] Bodhisatwa Sadhu, Member, IEEE, Mark A. Ferriss, Arun S. Natarajan, Soner Yaldiz, Member, IEEE, Jean-Olivier Plouchart, Senior Member, IEEE, Alexander V. Rylyakov, Alberto Valdes-Garcia, Benjamin D. Parker, Aydin Babakhani, Scott Reynolds, Xin Li, Senior Member, IEEE, Larry Pileggi, Fellow, IEEE, Ramesh Harjani, Fellow, IEEE, José A. Tierno, and Daniel Friedman, Member, IEEEA ---Linearized, Low-Phase-Noise VCO-Based 25-GHz PLL with Autonomic Biasing, VOL. 48, NO. 5, MAY 2013

[4] Luciano Severino de Paula, Eric Fabris, Sergio Bampi,
Altamiro Amadeu Susin,‖ A High Swing Low Power CMOS Differential Voltage-Controlled Ring Oscillator‖ in 2007 IEEE Computer Society Annual Symposium on VLSI(ISVLSI'07)


[6] To-Po Wang, —A k-band low power colpitts VCO with voltage to current positive feedback network in 0.18 μm CMOS,‖ in IEEE on Microwave and Wireless Components Letters, vol. 21, no. 4, April 2011, pp 218 – 220


